What we claim as our invention is:

1. An integrated circuit comprising:

a memory,

a digital signal processor coupled to said memory,

first and second direct memory access devices each coupled to said memory, and

a first sharing unit coupled to said memory and to said first and second direct memory access devices and adapted to alternately couple said first and said second direct memory access devices to said memory.

2. The integrated circuit of Claim 1, wherein:

said first and second direct memory access devices are programmable logic cores.

3. The integrated circuit of Claim 1, wherein:

said digital signal processor operates at a first clock frequency,

said first and second direct memory access devices operate at a second clock frequency slower than said first clock frequency.

4. The integrated circuit of Claim 3, wherein:

said second clock frequency is one-fourth of said first clock frequency and said first sharing unit alternates connection of said first and second direct memory access devices to said memory at a frequency of one-half of said first clock frequency.

5. An integrated circuit according to Claim 4, wherein:

said first clock frequency is 160 megahertz.

6. The integrated circuit of Claim 1, further comprising:

a memory controller coupled to said memory, to said digital signal processor and to said first sharing unit,

said memory controller adapted to, in response to a memory transaction request from a direct memory access device, provide a control signal indicating that the requested operation was done if there was no conflicting request from said digital signal processor and provide a control signal indicating that the requested operation was not done if there was a conflicting request from said digital signal processor.

7. The integrated circuit of Claim 1 further comprising;

a third direct memory access device coupled to said memory, and

a second sharing unit coupled to said memory, to said first sharing unit and to said third direct memory access device and adapted to alternately couple said first sharing unit and said third direct memory access device to said memory.

8. The integrated circuit of Claim 7 wherein:

said digital signal processor operates at a first clock frequency,

said third direct memory access device operates at a second clock frequency slower than said first clock frequency,

said first and second direct memory access devices operate at a third clock frequency slower than said second clock frequency.

9. The integrated circuit of Claim 8 wherein:

said second clock frequency is one-half said first clock frequency,

said third clock frequency is one-fourth of said first clock frequency,

said first sharing unit alternates connection of said first and second direct memory access devices to second sharing unit at a frequency of one-half of said first clock frequency, and

said second sharing unit alternates connection of said first sharing unit and said third direct memory access device to said memory at said first clock frequency.

10. An integrated circuit according to Claim 9, wherein:

said first clock frequency is 160 megahertz.

11. An integrated circuit comprising:

a digital signal processor operating at a first clock frequency and having an internal memory,

a first direct memory access device operating at a second clock frequency slower than said first clock frequency;

a second direct memory access device operating at a third clock frequency slower than said first clock frequency;

a first sharing unit having a first port coupled to the first direct memory access device, a second port coupled to the second direct memory access device, and a third port coupled to the digital signal processor internal memory, said first and second ports alternately coupled to said third port in synchronization with said first clock frequency.

12. An integrated circuit according to Claim 11, wherein:

said second clock frequency and said third clock frequency are each one-fourth of said first clock frequency and said first sharing unit alternates connection of said first and second ports to said third port at a frequency of one-half of said first clock frequency.

13. An integrated circuit according to Claim 11, wherein:

each of said first and second direct memory access devices is a programmable logic core.

14. An integrated circuit according to Claim 11, further including:

a third direct memory access device operating at a fourth clock frequency slower than said first clock frequency;

a second sharing unit having a first port coupled to the first sharing unit third port, a second port coupled to the third direct memory access device, and a third port coupled to the digital signal processor internal memory, one of said second sharing unit first and second ports alternately coupled to said second sharing unit third port in synchronization with said first clock frequency.

15. An integrated circuit according to Claim 14, wherein:

said fourth clock frequency is one half said first clock frequency,

said second clock frequency and said third clock frequency are each one-fourth of said first clock frequency,

said first sharing unit alternates connection of its first and second ports to its third port at a frequency of one-half of said first clock frequency, and

said second sharing unit alternates connection of its first and second ports to its third port at a frequency equal to said first clock frequency.

16. An integrated circuit according to Claim 15, wherein:

said first clock frequency is 160 megahertz.

17. An integrated circuit according to Claim 14, wherein:

said third direct memory access device is a programmable logic core.

18. An integrated circuit according to Claim 11, wherein:

said digital signal processor comprises a processor core, a memory and a memory controller,

said memory controller couples memory operations between said processor core and said memory and between said direct memory devices and said memory,

said memory controller, in response to a memory transaction request from a direct memory access device, provides a control signal indicating that the requested operation was done if there was no conflicting request from the processor core and provides a control signal indicating that the requested operation was not done if there was a conflicting request from the processor core.

19. A method for coupling a plurality of memory access devices to internal memory of a digital signal processor system, comprising:

sequentially coupling each of said memory access devices to said internal memory on a time-multiplexed basis, with the time allocation for each device based on the bandwidth of said memory access devices relative to the bandwidth of said internal memory.

20. A method for coupling two memory access devices to internal memory of a digital signal processor system, comprising:

coupling each of said two memory access devices to first and second ports of a multiplexor,

coupling a third port of said multiplexor to said internal memory of said digital signal processor system, and

alternately coupling said first and second ports of said multiplexor to said third port of said multiplexor in synchronization with a clock timing operations of said digital signal processor system.

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